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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Sadeg M. Faris)
) Group Art Unit
SERIAL NO.: Tbd) Tbd
)
FILING DATE: November 19, 2003) Examiner
) Tbd
FOR: Method of Fabricating Vertical Intergrated)
Circuits)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL of NEW PATENT APPLICATION UNDER 37 CFR 1.53

Sir:

Applicant is a small entity.

Please find enclosed herewith:

- 1) New Patent Application, including:
 - a. Specification (83 pages)
 - b. Claims (5 pages)
 - c. Abstract (1 page)
 - d. Figures (50 sheets)
- 2) Declaration and Power of Attorney (unexecuted)
- 3) Postcard

Respectfully submitted,

By: 

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Date: November 19, 2003
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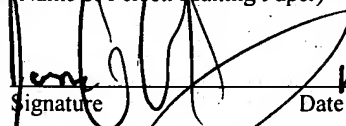
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